CLAIMS:

1. A frequency synthesizer including a phase-locked loop (10), which phase-locked loop (10) comprises:

- a frequency divider (14) having integral dividing ratios, connected between a voltage-controlled oscillator VCO (12) and a phase-frequency comparator PFD (16),
- a sigma-delta modulator (30), connected to the frequency divider (14) for commuting the dividing ratio of the frequency divider between a series of at least two integral values, so as to obtain a resulting mean dividing ratio with a fractional component, the modulator having at least a digital input (34, 50) suitable for receiving an adjusting instruction of the fractional component,

characterized in that the frequency synthesizer further includes:

- means for fixing the value of the least significant bit of the adjusting instruction to 1.

2. A synthesizer as claimed in claim 1, having an input (34) for a control value (K) of the fractional component, and in which the means for fixing the value of the least significant bit to 1 comprise means (52) for adding one bit equal to 1 to the control value (K) of the fractional component and thus for forming the adjusting instruction (K') applied to the sigma-delta modulator.

3. A synthesizer as claimed in claim 2, comprising an input register of rank L-1, where L is an integer, and in which the means for adding a bit equal to 1 comprise an instruction register of rank L, a locked flip-flop (52) for setting the least significant bit of the register of rank L to 1 and means for copying the control value in the instruction register of rank L as most significant bits.

4. A synthesizer as claimed in claim 1, comprising an input register which has a control value (K) of the fractional component, in which the means for setting the value of the least significant bit of the adjusting instruction to 1 comprise means for replacing the least

significant bit of the control value by the value 1 and for applying this value to the modulator as an adjusting instruction.

5. A frequency synthesizer as claimed in claim 1, in which the sigma-delta modulator is a two-stage modulator.

6. A synthesizer as claimed in claim 1, further including at least a frequency divider (100) having a set fractional dividing ratio, the divider (100) being connected between the voltage-controlled oscillator VCO (12) and the frequency divider (14) having integral dividing ratios, and means (40, 102) for activating the frequency divider having a fractional dividing ratio when the fractional component (k) of the mean dividing ratio is contained in at least a given range of values, and for modifying in a corresponding manner the adjusting instruction of the fractional component of the sigma-delta modulator to keep a rough dividing ratio unchanged of the frequency divider having a fractional dividing ratio, the latter divider being associated to the frequency divider that has integral dividing ratios.

7. A synthesizer as claimed in claim 6, in which the value ranges of the fractional component k, such as $0 < k < 0.25$ and $0.75 < k < 1$, correspond to activation ranges of the frequency divider (100) which has a fractional dividing ratio.

8. A synthesizer as claimed in claim 7, in which the divider having fractional dividing ratios is a divide-by-1.5 divider.

9. A method of synthesizing frequency by means of a phase locking synthesizer, comprising:

- a frequency divider (14) having integral dividing ratios, connected between a voltage-controlled oscillator VCO (12) and a phase-frequency comparator PFD (16),
- a sigma-delta modulator (30), connected to the frequency divider for commuting the dividing ratio of the frequency divider between a series of at least two integral values so as to obtain a resulting mean dividing ratio that has a fractional component, the modulator having a digital input for an adjusting instruction of the fractional component, and according to which an adjusting instruction is formed for the sigma-delta modulator via a modification of a control input value, the input value being modified to make it an odd value.

10. A method as claimed in claim 9, in which a least significant bit of the control input value is modified to make it equal to 1.

11. A method as claimed in claim 9, in which a least significant bit, equal to 1, is added to the control input value to form the adjusting instruction.

12. A frequency synthesizing method as claimed in claim 9, by means of a frequency synthesizer which further includes at least a frequency divider (100) having a fixed fractional dividing ratio, connected between the voltage-controlled oscillator (12) and the frequency divider (14) having integral dividing ratios, in which method said frequency divider having fractional dividing ratios is activated when the fractional component (k) of the dividing ratio is contained in at least a given range of values and the adjusting instruction of the fractional component of the sigma-delta modulator is modified in corresponding manner to keep a rough dividing ratio unchanged of the frequency divider having a fractional dividing ratio, the latter divider being associated to the frequency divider that has integral dividing ratios.

13. A method as claimed in claim 12, in which said frequency divider having a fractional dividing ratio is activated when the fractional component k of the dividing ratio is such that $0 < k < 0.25$ or $0.75 < k < 1$, and said frequency divider having a fractional dividing ratio is deactivated when the fractional component k of the dividing ratio is such that $0.25 \leq k \leq 0.75$.

14. A frequency converter comprising a mixer (200) which has a first input connected to a signal source which delivers a signal with a frequency to be converted, and comprising a signal source (1) which has a reference frequency connected to a second input of the mixer, characterized in that the signal source (1) which has a reference frequency comprises a frequency synthesizer as claimed in any one of the preceding claims.

15. A use of a frequency converter as claimed in claim 14 in a portable telephone.